RESEARCH DEPARTMENT

New equipment for the statistical analysis of sound programme levels

TECHNOLOGICAL REPORT No. L-070

UDC 534.86:
621.317.326

1966/65

THE BRITISH BROADCASTING CORPORATION
ENGINEERING DIVISION

RESEARCH DEPARTMENT

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CORRIGENDA

RESEARCH DEPARTMENT - BRITISH BROADCASTING CORPORATION

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Page 4:

The caption to Fig. 4 should read:

"Schematic diagram of Programme Level Analyser operating as a constant rate sampler".

Page 7:

In Fig. 6, transformer ARD 615C secondary voltages should be 36·5V not 365V.

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NEW EQUIPMENT FOR THE STATISTICAL ANALYSIS OF SOUND PROGRAMME LEVELS

SUMMARY

The report describes apparatus for the statistical analysis of programme level fluctuations. The equipment, which is transistorized and self contained, can be used either for counting and classifying programme peaks or for analysing the levels on a percentage time basis, functions previously performed by two separate and now obsolete devices.

The new equipment is free from some of the limitations of its predecessors and its performance is adequate for all applications at present envisaged.

1. INTRODUCTION

Investigations involving the statistical analysis of programme levels have for 15 years been carried out using locally-constructed apparatus of a relatively crude kind.[1] Two pieces of equipment have been used for this work, both of them deriving their input signals from the current supplied by a standard peak programme meter amplifier and registering data on a series of electromechanical counters. One of these devices indicates the number of programme peaks exceeding specified voltage levels; the other samples the signal at regular time intervals and registers the proportion of the total time during which the voltage exceeds certain specified levels.

The instrument to be described was designed to replace the two ageing pieces of apparatus described above and to provide improved performance and wide range of measurement both in terms of voltage level and counting rate. It is self-contained, mains operated and can be used for the analysis of signal levels between -20 dBm to + 10 dBm. Fig. 1 shows a general view of the equipment.

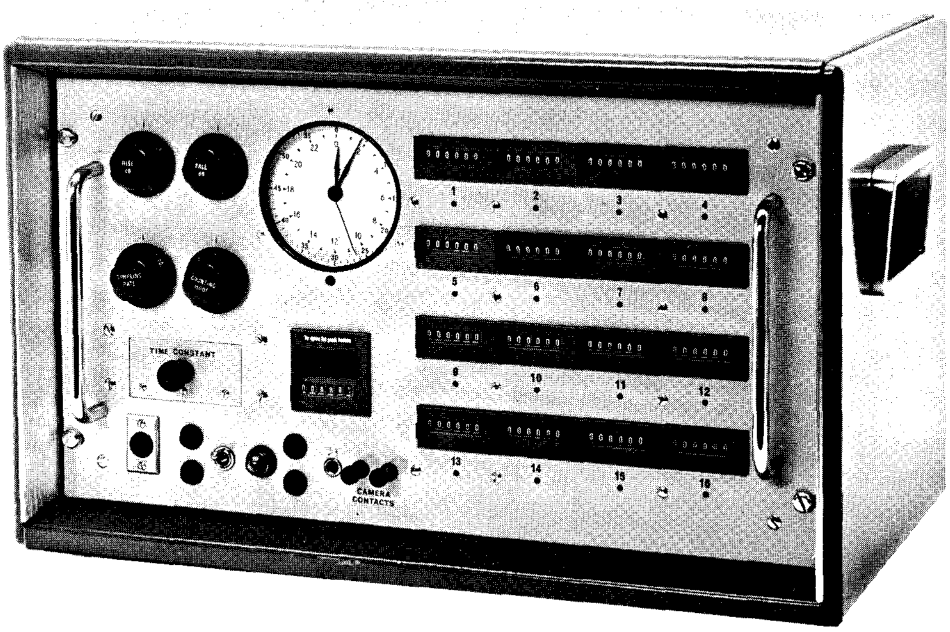

Fig. 1 - Programme Level Analyser: General appearance.

2. DESIGN CRITERIA

The old equipment provided for the analysis of programme exceeding five voltage levels only. This number of voltage classes has been found to be inconveniently small for many purposes. For recorded programmes which can be replayed at will at any required level, five voltage classes are sufficient to define the form of distribution of programme voltages with fair accuracy, but for live material, over which no preliminary control can be exercised, much important information can be lost. In order to provide data on the distribution of programme voltages over the desired level range, which is estimated at 30 dB, the new equipment has been made to provide 16 voltage classes at 2 dB intervals. The choice of 2 dB for class width has been shown by operating experience with the earlier equipment to provide a satisfactory compromise between unnecessary complexity on the one hand and inadequate discrimination on the other.

The maximum speed of operation of the old counting equipment was about five counts per second, the limit being imposed by the addition of a number of time constants within the equipment. In practice, however, the instrument was set to ignore peaks of height less than 3 dB; since the maximum rate of fall of the programme meter current is 8·7 dB/sec, it was impossible for more than three such peaks to occur in one second. The new counting equipment is intended to be more versatile than the old and to operate with a faster return time constant if required. To this end provision is made for registering up to 25 counts per second; this higher speed will allow more detailed analysis of such phenomena as the transient performance of limiters and the level distribution of intermittent noise, interference or even of distortion. Further, if the high counting speed is undesirable for some particular purpose, the count rate can be controlled by an electrical time constant, easily adjustable by the user.

The equipment is designed to work unattended if required and to provide a control signal for an electrically-operated camera to photograph the counters, either at regular time intervals or after a prescribed number of counts.

A complete circuit diagram of the apparatus is shown in Fig. 6; a number of considerations affecting the detailed design of the equipment are discussed in the Appendix.

The following sections describe the operation of the instrument as a peak counter and as a constant-rate sampler.

3. PEAK COUNTING

A schematic diagram of the programme level analyser operating as a peak counter is shown in Fig. 2, to which reference should be made during the reading of the following sub-sections. Fig. 3 shows an example of the voltages appearing at various parts of the system during one complete cycle of operation.

The input signal to the analyser passes via a buffer amplifier to a signal rectifier. The charge and discharge time constants of the associated smoothing circuit are under the control of the operator. From the time constant circuit one output is applied to the 'peak memory and voltage level classifier' which provides priming signals to appropriate 'AND' gates whenever the programme voltage level exceeds each one of the sixteen set levels.

Since a signal peak cannot be counted until it has been followed by a fall in amplitude, the voltage level classifier is provided with a memory to retain the peak voltage value until the count is made.

The other output from the time constant circuit operates a system of units, shown enclosed in the dotted box in Fig. 2, the function of which is the recognition of programme voltage peaks. The recognition of a programme voltage peak by the above assembly results in a pulse being applied to the second input of all the 'AND' gates. The simultaneous presence of signals at both inputs causes each 'AND' gate to actuate its associated counter.

The conditions which must be met to define the occurrence of a peak in the programme level are that a certain minimum increase in level must have occurred since the last trough, that the signal voltage should cease to increase and should then fall by at least a specified amount. In this connection a specified amount should be understood to be a specified percentage of the signal voltage, i.e. a fixed number of decibels, since programme measurements are normally made in logarithmic units. For this reason, the signal, on entering the peak recognizing system, is passed through a circuit producing an output proportional, over the working range, to the logarithm of the input, and referred to for brevity as a 'logarizer'. Outputs from the logarizer are applied to peak and trough memory circuits, which register respectively the maximum and minimum values of logarizer output voltage.

The output from the trough memory is continuously compared with the output from the logarizer by the 'rise difference detector' and whenever the

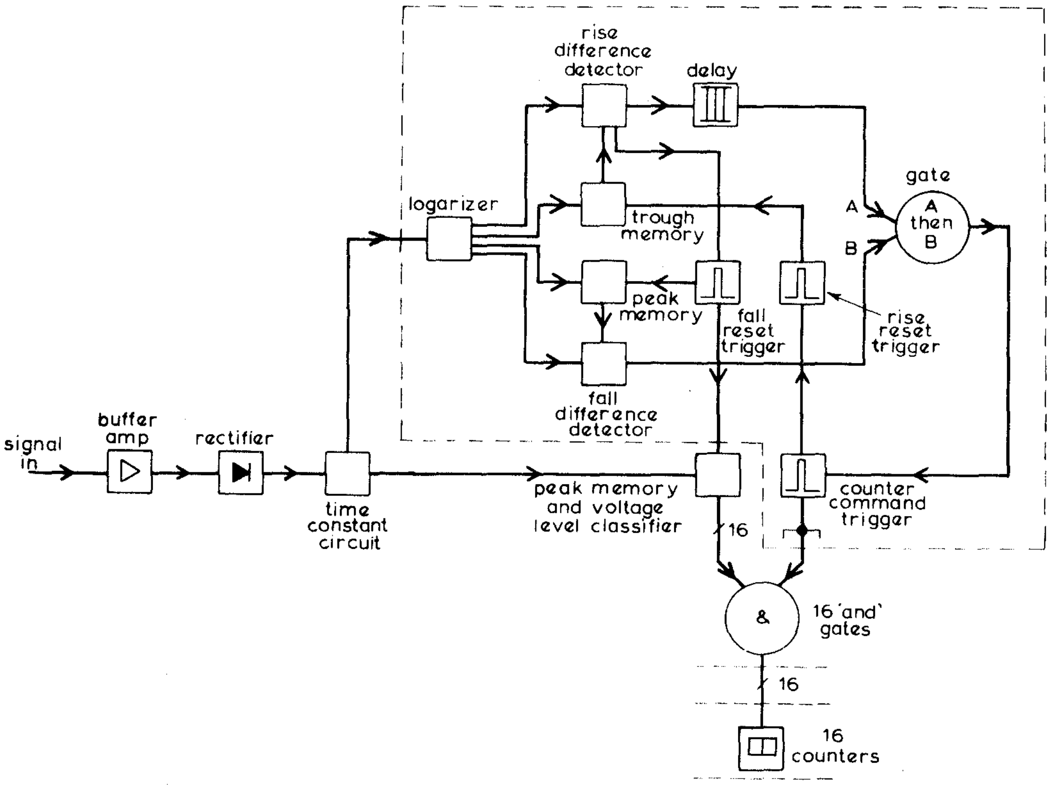

Fig. 2 - Schematic diagram of Programme Level Analyser operating as a peak counter.

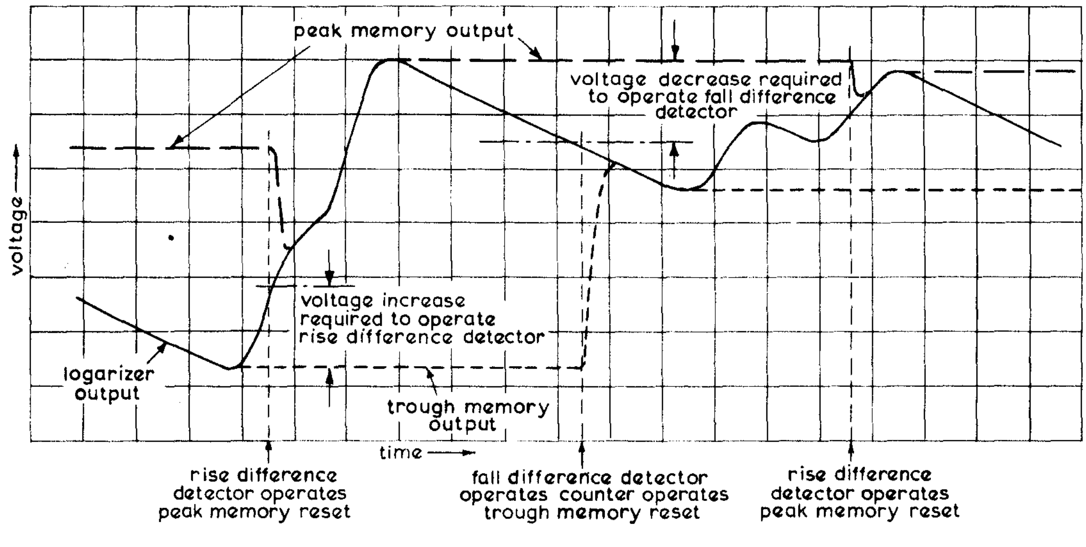

Fig. 3 - Operating cycle of peak recognizing system.

difference between these two outputs exceeds a prescribed value, a signal is applied through a delay circuit (the purpose of which will be apparent later) to one input, 'A', of a switching unit referred to as an 'A' then 'B' gate.* Similarly, the output from the peak memory unit is continuously compared with the output from the logarizer by the fall difference detector and the difference, if large enough, results in a signal being applied to the 'B' input of the 'A then B' gate. Thus, whenever a peak occurs, signals are applied to both inputs of the 'A then B' gate which then fires the 'counter command trigger'; this in turn provides the second input to the counter 'AND' gates and actuates the counters.

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* The 'A then B' gate is a two-input one-output gate which opens whenever a signal is applied to the 'A' input and is later joined by a signal applied to the 'B' input. The gate remains closed if the 'B' input signal arrives first.

Some further details concerning the operation of the peak recognizing system require mention to complete the explanation.

(a) In recognizing a peak as a rise of signal level followed by a fall, the correct time sequence of these events is essential. It is necessary to ensure that a fall followed by a rise, i.e. a trough, is not accidentally counted as a peak. To this end, the output from the 'rise difference detector' is arranged to operate the 'fall reset trigger' unit; this in turn resets the 'peak memory', thus cancelling information about the previous fall. After a peak is counted the information about the previous rise, which still remains in the 'trough memory', must be cancelled. In this case, however, the cancellation is brought about by the operation of the 'counter command trigger', thus ensuring that the rise information cannot be destroyed before the count is completed.

(b) The delay circuit in the 'A' input to the 'A then B' gate, to which reference has already been made, is necessary to prevent simultaneous appearance of both inputs to the gate at the moment when the rise signal associated with a trough cancels the fall signal associated with a trough cancels the fall signal associated with the previous peak. The actual circuit of the 'A then B' gate linking the 'rise and fall detectors' to the 'counter command trigger' is in fact that of a simple 'AND' gate. The 'A then B' action is achieved by the resetting arrangements in conjunction with the delay circuit, which ensure that the 'B' pulse cannot effectively precede the 'A' pulse.

4. CONSTANT-RATE SAMPLING

Fig. 4 shows a schematic diagram of the Programme Level Analyser operating as a constant-rate sampler. The buffer amplifier, rectifier, time constant circuit and level classifier are the same as those employed for peak counting, but for the present purpose the level classifier is operated without a memory. The remaining input for each of the 'AND' gates is provided by a 'clock pulse oscillator' which controls a pulse generator to provide gating pulses locked to the oscillator frequency. At the instant when a gating pulse arrives, all counters already receiving a signal from the 'voltage level classifier' make one count. It is essential for this type of measurement that the gating pulse width shall not greatly exceed the minimum required to operate the counters. If the gating pulse is present at the 'AND' gate for a considerable part of the sampling period, a momentary reduction of the programme level can cause a spurious count to be registered. Under these conditions the units of time set by the gating pulse repetition rate become sub-divided and the subdivisions may be counted in error as if they were whole units.

A totalling counter is provided to register the number of gating pulses, which is proportional to the total time elapsed since the commencement of the measurement.

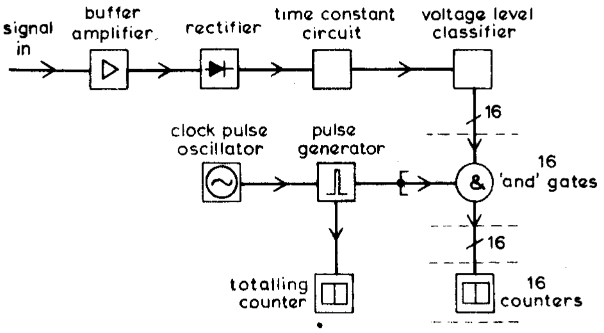

Fig. 4 - Schematic diagram of Programme Level Analyser operating as a ~~peak counter~~ constant rate sampler.

5. PERFORMANCE

5.1 Frequency characteristics

Fig. 5 shows the variation of signal rectifier output voltage as a function of input frequency. The output relative to the 1 kHz value falls by 0·3 dB at 40 Hz and rises by 0·3 dB at 20 kHz.

5.2 Accuracy of voltage levels

The individual counter operating levels are adjustable by approximately ± 1 dB about the 2 dB spacings for which the instrument was designed. The adjustment can readily be made to within ± 0·2 dB and this accuracy is maintained over several days.

5.3 Maximum Speed of Counting

The manufacturer's rated maximum speed for the mechanical counters employed is 25 counts per second and the electronic circuit was designed accordingly.

Reliable peak counting has been achieved on pulses of 1 kHz tone up to 21·8 counts per second using a suitably short signal rectifier time constant, the maximum counting rate being limited by the tone-pulsing equipment with which the test was conducted.

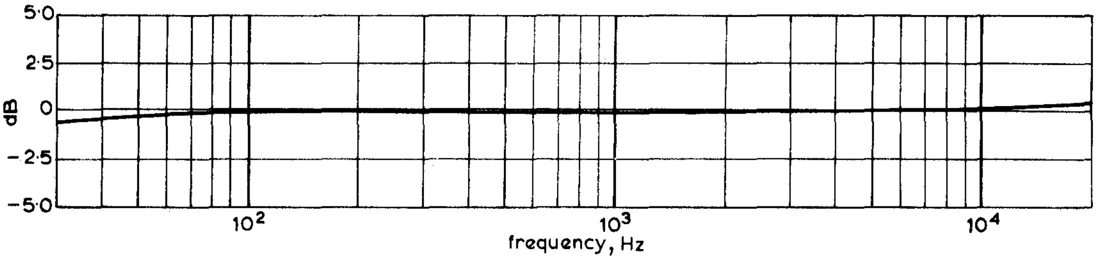

Fig - 5 Programme Level Analyser: frequency characteristic.

5.4 Minimum Speed of Counting

Since peak and trough values of programme voltage have to be stored in charged capacitors, it follows that there will be a maximum time for which the information can be retained. Narrow pulses of programme widely spaced in time present no problem because the rise information has to be stored only for the length of the pulse. The most severe requirements fall upon the trough memory for programme signals which maintain a constant amplitude for a long time. The trough memory voltage drifts at a rate of approximately 0·6 dB per second. The effect of this drift can be illustrated by considering the case of a signal consisting of a continuous tone, the level of which is alternately raised and lowered for equal time intervals by the intermittent introduction of a 3 dB attenuator. If, for example, the equipment is adjusted to make the 'rise difference detector' operate with a 1½ dB increase in signal level, these level changes will not be registered if their repetition frequency is less than 11 per minute. The design of the trough memory circuit is controlled by the conflicting requirements of short charge time on fast counting and long discharge time on slow counting, and although the trough memory could be improved to deal with extremely slowly changing voltages, it would be at some sacrifice in fast counting rate or alternatively at the expense of greater circuit complication.

6. CONCLUSION

The apparatus described above has been in intermittent use, over a period of about a year, in connection with various investigations involving the analysis of programme level fluctuations, and continues to function satisfactorily.

7. REFERENCE

1. Peak counting and integrating circuits for the statistical analysis of programme levels. Research Department Technical Memorandum No. L-1004.

APPENDIX

Fig. 6 shows the circuit diagram of the complete equipment. For simplicity only one of the sixteen identical level classifying 'AND' gates is shown.

The input amplifier, comprising transistors TR1 to TR4, is a conventional push-pull stage having about 40 dB of negative voltage feedback. The output transformer provides the following full-wave peak rectifier with alternating voltages up to 30 volts peak and currents up to 30 mA peak, the effective source impedance being approximately 70 ohms.

The signal rectifier charge and discharge time constant components R_C, C and R_D can be readily changed as required. The current capability of the preceding amplifier permits of R_C being made as low as 1 kΩ without overload upon sudden application of maximum signal. The rectified voltage across the smoothing condenser C is applied to the paired emitter-follower TR5, TR6. The input resistance of TR5 is approximately 50 MΩ so that its shunting effect need only be considered for values of R_D greater than say 5 MΩ.

The output from TR6 is applied to the level classifier and also to the logarizer. The signal voltage for the level classifier is taken via a peak memory circuit consisting of a rectifier and capacitor, and the paired emitter follower TR7, TR8 when the instrument is counting peaks, and via a by-pass circuit for Constant Rate Sampling (C.R.S.). In the latter case, two diodes OA202 are used to simulate the base-emitter voltage offsets of TR7, TR8 so that no d.c. shift occurs in the apparatus when these transistors are bypassed. The signal voltage range throughout the equipment is taken as -25 to -5 volts with respect to earth. This range of signal voltage was chosen to be comfortably within the -30 volt supply, leaving a margin of 5 volts at each end of the range to ensure linear operation of the transistors. Since the level classifier is not logarized, logarithmic spacing of the levels representing the class boundaries would result in the first eight counters being crowded within the first 3·5 volts of the 20 volt total range. To spread these counting levels over a larger voltage range, a d.c. amplifier, TR15 and TR16, having a voltage gain of 5, is inserted in the signal line feeding the first eight counters. This d.c. amplifier is designed to have an offset zero such that when the input is +5 volts relative to the negative line the output voltage is also +5 volts.

Signals arriving from the d.c. amplifier or direct from point A, according to the level range, are applied to the level classifying 'AND' gates, a typical specimen of which, employing transistors TR50, TR51 and TR52, is shown in the circuit diagram. Until the input signal to TR51 reaches a pre-set level, TR52 conducts; when this voltage level is exceeded the standing emitter current is transferred from TR52 to TR51. On the occurrence of a peak, a signal from the peak recognizing equipment (from point B) cuts off TR50. When TR52 and TR50 are both cut off, TR53 is bottomed and the counter CTR1 is connected across the 50 volt supply. The diode in parallel with the counter coil avoids possible damage to TR53 through the inductive voltage surge, which would otherwise develop when the current is interrupted.

The first unit in the peak recognizing equipment is the logarizer, which consists of a ladder attenuator having biassed diodes in the shunt circuits; it is followed by a d.c. amplifier, TR17, TR18 and TR19, to recover the original voltage level range. As with the d.c. amplifier used to drive the level classifiers, an offset zero is arranged so that the signal starting point both for input and output shall be +5 volts relative to the −30 volt line.

From TR19 the signal divides into four paths via emitter followers TR20, TR21, TR22 and TR23. Signals from TR22 and TR21 are passed respectively to one input of the rise difference detector TR28, TR27 and TR29, and to the trough voltage memory, consisting of a rectifier and capacitor followed by TR24, TR25 and TR26. The trough voltage memory output plus an offset voltage selected by the 2·5 kΩ 'Set Rise' potentiometer in the emitter circuit of TR25 is applied to the other input of the rise difference detector. When the base of TR28 is more positive than that of TR27 (a state of affairs which occurs whenever the prescribed rise in signal level has been achieved) current is transferred from TR27 to TR28 and a pulse of voltage appears across the 1 kΩ resistor in the collector circuit of TR28. The amplitude of this pulse, 5 volts, is independent of the absolute value of signal voltage because TR29 is biassed to produce a constant current (5 mA). In order that the voltages appearing at the emitters of TR22 and TR25 when the signal is passing through a minimum should be equal, it is necessary that the voltages applied to the bases of TR21 and TR22 be offset to allow for the various base-emitter and diode volt drops in the circuit. To this end the chain of forward biassed diodes in the emitter feed

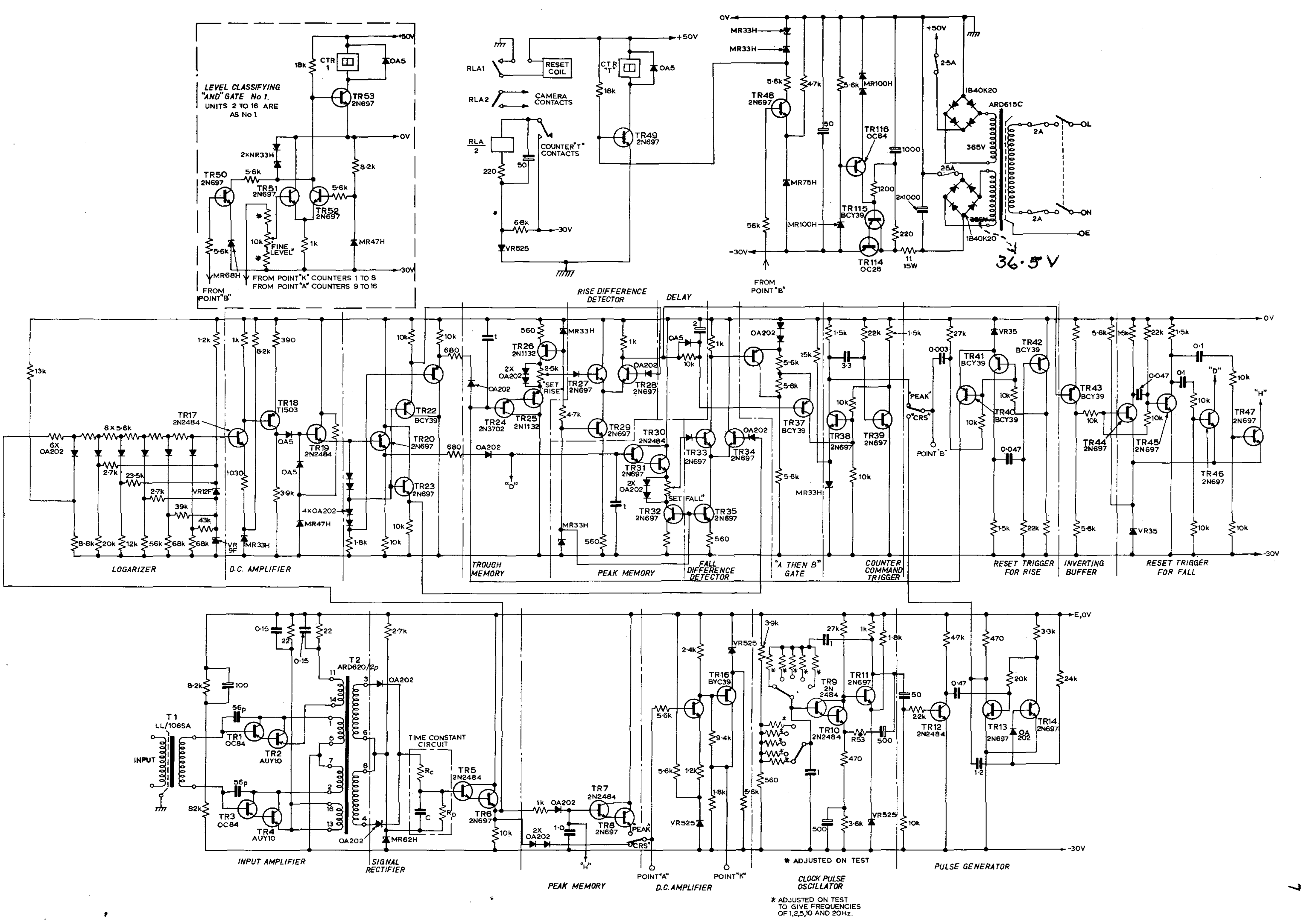

Fig. 6 - Programme Level Analyser: complete circuit.

to TR19 provides a number of voltage taps spaced at approximately 0·6V intervals, 0·6V being the knee voltage of the diodes, irrespective of the absolute value of the signal voltage.

Signals from TR19 applied to transistors TR20 and TR23 are passed respectively to a peak memory circuit consisting of a rectifier and capacitor, followed by transistors TR30, TR31 and TR32, and to the fall difference detector TR33, TR34 and TR35, where by reasoning similar to that employed in the case of the rise difference detector, they can be seen to produce an output pulse at the collector or TR33 whenever the prescribed fall in signal level occurs.

The diodes in series with the bases of the 2N697 transistors TR27, TR28, TR33 and TR34 are required because the maximum permitted reverse base voltage is 6 volts, considerably less than the signal voltage swing. Without the protection of these diodes, a large difference between the instantaneous signal value and the appropriate memory voltage could lead to the destruction of the transistor concerned.

Transistors TR36 and TR37 form an 'A then B' gate connecting the outputs of the rise and fall difference detectors to the counter command trigger. The presence of an output pulse from TR33 at the base of TR36 bottoms TR36 and reduces the emitter bias on TR37 from approximately −10V to approximately −1·2V with respect to earth. If an output pulse from TR28 is already present, at the base of TR37, TR37 also bottoms and the resulting pulse applied to the base of TR38 operates the counter command trigger TR38 and TR39, thus firing the appropriate counters.

Resetting peak and trough memories is accomplished by monostable trigger circuits employing transistors TR41, TR42, TR44 and TR45, which shunt the appropriate memory capacitors through transistors TR40, TR46 and TR47. The currents in the shunting transistors are sufficient to override the charging currents entering the capacitor and to discharge the latter in less than 1 ms. The reset trigger for the fall, using npn transistors, requires an inverting buffer amplifier TR43 to drive it in order to provide a positive-going pulse relative to the main negative supply line.

The counter 'T', driven through transistors TR48 and TR49 records the total number of clock pulses for Constant Rate Sampling or the total number of peaks when peak counting.

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